# DOE relates Spring Probe Variables to Signal Integrity

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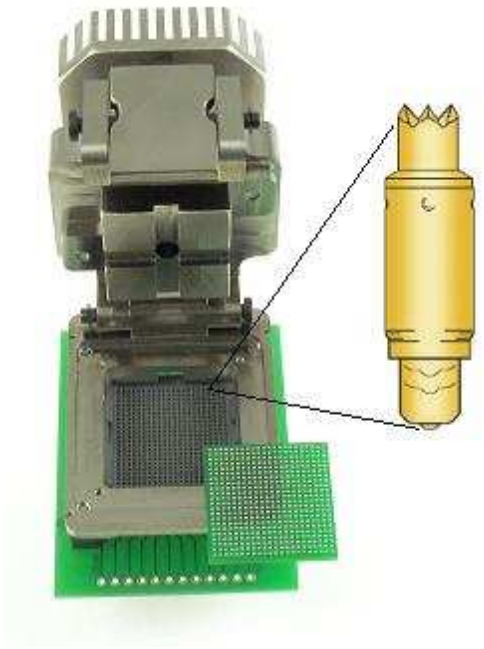

Figure 1: Spring pin socket showing features of spring probe contact

**Introduction**

One of the modern world's driving engines is the semiconductor also referred to as the IC (Integrated Circuits). These ICs are fabricated, assembled and tested in billions of units every year. The semiconductor industry is being driven by the mantra "small, fast and cheap". Testing challenges grow largely due to smaller size and faster performance (bandwidth) of IC devices. The socket industry that enables testing of semiconductor devices is heavily taxed by smaller and faster devices in addition to the other supporting segments of the semiconductor market. IC device manufacturers and test houses require reliable socket solutions for these high performance devices. Smaller and faster devices are typically more sensitive to changes in the electrical configurations used for testing, particularly in the case of AC performance often referred as "signal integrity".

**Automatic Test Equipment System**

A typical test system includes hardware and software to run different tests to validate the performance of an IC. Test systems can be categorized as consisting of four distinct components – tester, load board, test socket, and handler. The test socket is mounted to the load board, which in turn is interfaced to the tester. A handler includes compartments for trays where DUTs (devices under test) are stored. A vacuum head/plunger inside the handler inserts the DUT into the test socket (bringing the IC contacts together with the test socket contactors) while the tester component performs the necessary tests. If we think of a test socket as the 'heart' of an ATE (Automatic Test Equipment) system then the spring probes are the 'arteries' that transfer the signal from the device under test to the tester through the load board. The health of these spring probes is essential to the performance of the test socket – but how do we test the spring probes or rate their health?

**Signal Integrity**

Insertion loss of the spring probe is one of the first parameters verified by the electrical test engineer. This determines whether the socket / interconnect system will pass the functional test of devices. There are seven principles for Optimized Insertion Loss mentioned by Eric Bogatin *[BiTS 2005 Signal Integrity of Test Sockets – Simplified, page 32]* which are listed below.

1. Match the characteristic impedance of the socket to 50 Ohms
2. Keep the impedance constant through the socket
3. Optimize (minimize) pad stack up capacitance
4. Keep the socket contacts short
5. The dielectric loss of the socket is not critical
6. The conductor loss of the socket is not critical
7. The contact resistance of the socket is not critical

Spring pins are a common interconnect medium used in the socket (**Figure 1**) and there is no established relation between critical spring probe parameters and their influence on signal integrity other than keeping those contacts short. There is no baseline reference (or starting point) for spring probe design which is an everyday need due to emerging new application requirements because of the varying functionality of IC devices. For example, an IC with a data rate of 5Gbit/s requires a bandwidth of 2.5GHz. And when functions are extended to 3$^{rd}$ or 5$^{th}$ harmonics, depending upon the requirement, a corresponding bandwidth of 7.5GHz or 12.5GHz is needed. One way to accomplish this requirement is to over design a spring probe by making it extremely short which means compromising mechanical features for electrical superiority. In addition to electrically testing the IC devices, the spring probes needs to repeat the test for millions of IC devices. This can mean mechanical features become as critical as the electrical requirements. How can one strike a balance between electrical requirements and mechanical features?

**Design of Experiment**

This following paragraph demonstrates development of a model using DOE (Design of Experiment) to identify the optimized frequency without compromising mechanical features. To develop a model, the first step was to design a set of experiments by identifying key input factors and output responses. In our experiment, we used spring pin length, width and the ground pattern as input variables. We defined bandwidth as our output parameter for each experiment. Spring pin length was varied from 1mm to 4mm while spring pin diameter was varied from 0.25mm to 0.35mm. We used two ground patterns in our experiment. The first configuration was the typical 'G-S-G' and the second employed ground pins surrounding the signal pins in all four directions. Pitch was kept constant at 0.5mm. Full factorial design with 2 levels for each factor resulted in 8 experimental runs. Blocks were not used as the experiment is not dependant on the time factor. **Figure 2** shows run order, input variables and the output variable.

| Standard Order | Run Order | Block | Diameter (mm) | Length (mm) | Ground pattern | Bandwidth (GHz) |
|---|---|---|---|---|---|---|
| 7 | 1 | Block 1 | 0.25 | 4 | C2 | 14 |
| 4 | 2 | Block 1 | 0.35 | 4 | C1 | 5.6 |
| 3 | 3 | Block 1 | 0.25 | 4 | C1 | 13.9 |
| 8 | 4 | Block 1 | 0.35 | 4 | C2 | 4 |
| 5 | 5 | Block 1 | 0.25 | 1 | C2 | 31 |
| 6 | 6 | Block 1 | 0.35 | 1 | C2 | 14.8 |
| 2 | 7 | Block 1 | 0.35 | 1 | C1 | 19 |
| 1 | 8 | Block 1 | 0.25 | 1 | C1 | 33 |

Figure 2: Design of Experiments table showing run order, input variables and the output variable

**Statistical Model**

After running experiments, results were analyzed using DOE software. The first step in analyzing the data was to identify which input variables and their interactions had significant influence on the output variable. Typically, half normal plot and pareto charts are used to separate the significant variables from the insignificant ones. From **Figure 3**, it can be seen clearly that spring pin length had the ultimate effect on bandwidth, followed by spring pin diameter.

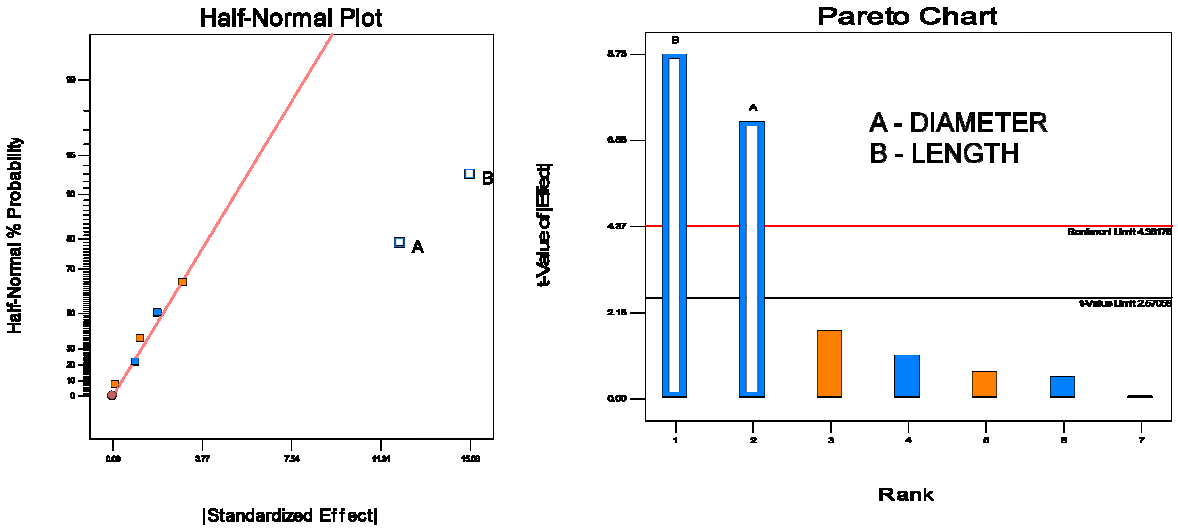


Figure 3: Half normal plot and Pareto charts showing the significant input factors from the insignificant ones

These are known as 'main effects'. The ground pattern did not have any influence on the bandwidth and so does the interaction of input variables. The next step was to generate an equation using these two input variables. DOE software presents this model through regression analysis.

**Bandwidth = 65.85 - 121.25 * Diameter - 5.025 * Length.**

**Analysis of Variance**

The above equation is valid within the limits used in our experiments (spring pin length from 1mm to 4mm and spring pin diameter from 0.25mm to 0.35mm). The next step is to verify the validity of the model using analysis of the variance function (ANOVA) in the DOE software. The Model F-value of 62.78 generated by ANOVA implies the model is significant. There is always a question of error percentage. There is only a 0.03% chance that a "Model F-Value" this large could occur due to noise. "Prob > F" value is less than 0.05 which indicates that the model terms are significant with a 95% confidence interval criteria. In this case, spring pin length and diameter are significant model terms. Values greater than 0.1 indicate the model terms are not significant (i.e. ground pattern and other interactions between input variables). Another factor used to validate the model is R-square (correlation factor). The maximum correlation is 1.00. In our case, the R-square value is 0.96 which means the model is very much coherent with the experimental data.

**Model Validation**

After developing the model and determining the relationship of spring pin length and diameter to bandwidth, the next step was to verify the model through experimentation. The main objective was to maximize spring pin bandwidth. Once this criterion was set in the DOE software, many solutions were found. The selected solution for our experiment recommended 1mm long and 0.25mm diameter spring pins with the G-S-G pattern. The software

also predicted the output bandwidth to be 30.5 GHz with a desirability of this outcome at 91%. The experiment was run using the selected solution variables and the results are shown in **Figure 4**.

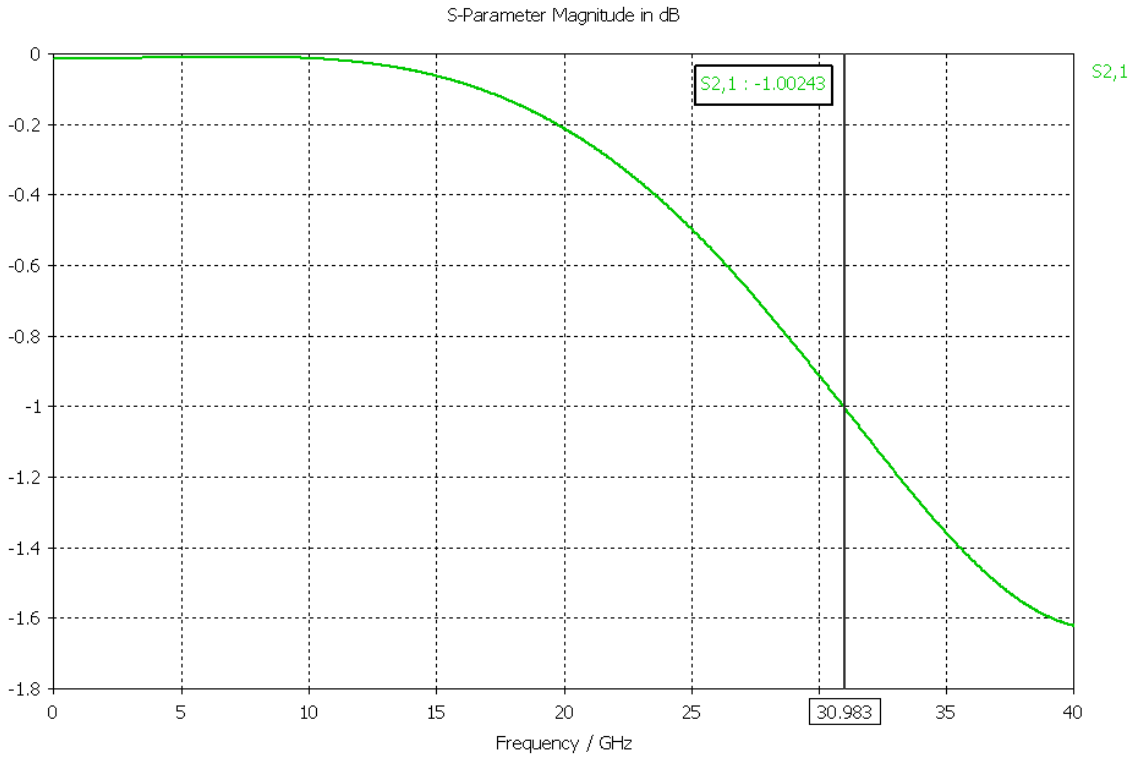


**Figure 4: Maximum bandwidth criteria represented in frequency versus insertion loss graph**

From the graph, it can be seen that the insertion loss of -1dB = 30.9GHz. This frequency is within 1.3% of the predicted value of 30.5GHz. The verification experiment proved the model was valid.

In order to be sure, a second experiment was planned to verify the model. We chose two parameters optimization. In this case, the main objective was to maximize both spring pin bandwidth and spring pin length. Maximizing spring pin bandwidth and spring pin length gains a mechanical advantage without losing electrical requirements. Maximum pin length (and thus a maximum spring length) ensures proper contact force. This 'must have' feature in direct correlation to DC resistance also suits better interconnect compliance. Target PCBs need more compliance to accommodate co-planarity variations due to mask thickness or plating thickness variations. IC devices with warpage, ball height variation also need more compliance to engage all pins, leads or balls. Once this criterion of maximum spring pin bandwidth and maximum spring pin length was set in the DOE software, many solutions were found. The selected solution for our experiment recommended 0.25mm diameter and 3.64mm long spring pins with a ground pattern around all signal pins. The software also predicted the output bandwidth to be 17.25 GHz with a desirability of this outcome at only 63%. Then the experiment was run using the selected solution variables and the results were shown in **Figure 5**. From the graph, it can be seen that the insertion loss of -1dB = 15.2GHz. This frequency was within 12% of the predicted value of 17.25GHz. Since the model cautioned that the desirability was only 63%, the actual result has to be used with a proper safety margin. The second experimental run also proved the model was valid (with proper precautionary measures).

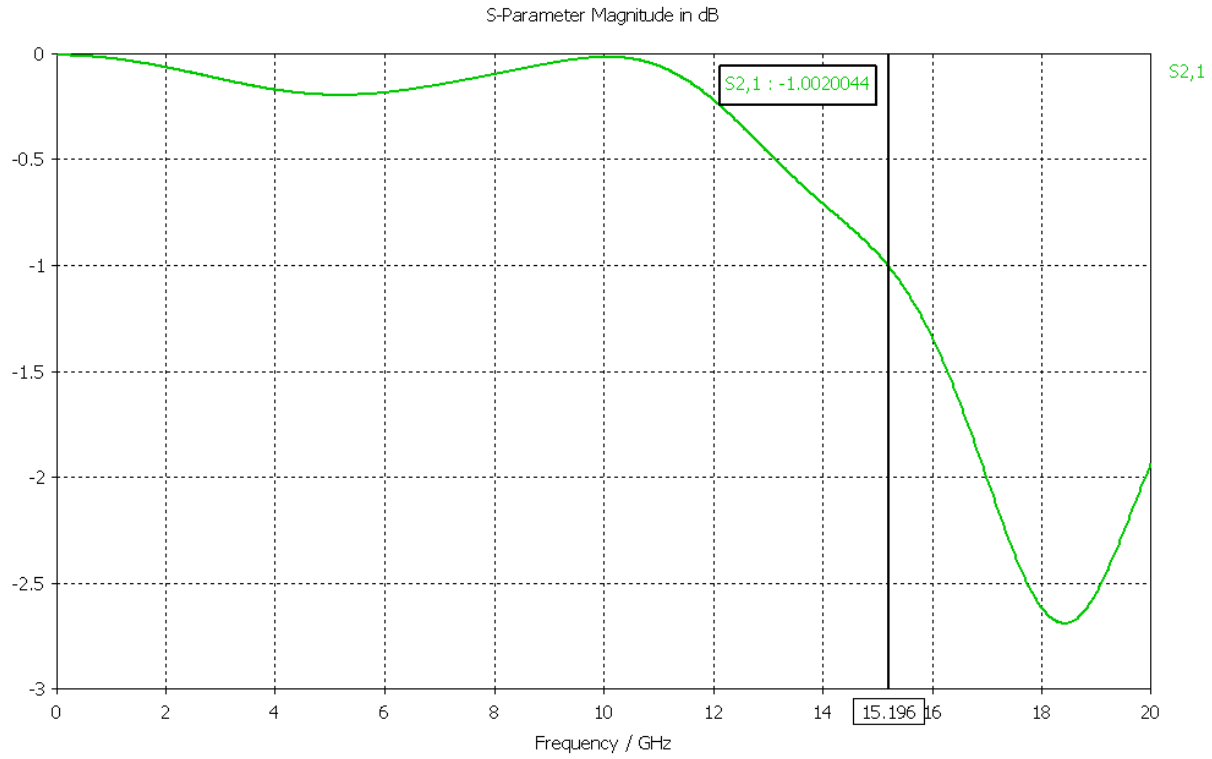


Figure 5: Maximum bandwidth and maximum length criteria represented in frequency versus insertion loss graph

**Conclusion**

This modeling technique can be extended with more input variables as well as output variables. The method allows one to choose which input variables will have significant influence on the output variables. This means insignificant variables need not be tightly controlled. This will make a significant difference in manufacturing and the yield can be improved to a higher sigma level – Design For Manufacturability. The model serves as a baseline reference and starting point for any spring probe design. By establishing relationships between critical spring probe parameters and their influence on signal integrity, the design cycle of new spring probes is reduced to coincide with a test process. Caution has to be exercised when using the model with its boundary conditions and one must understand the desirability of outcome. For example, spring pin length has to be between 1mm and 4mm and spring pin diameter has to be between 0.25mm and 0.35mm. By going through this statistical modeling, we identified that 'keeping it short' in addition to 'keeping it skinny' are must have spring pin features for optimized frequency characteristics in semiconductor test applications. Future work will include more spring pin variables such as plating, tip geometry, spring force as input factors and include mechanical life of spring probe in addition to electrical requirements as output factor. This will enable both mechanically and electrically optimized solution for semiconductor test applications.

**Author**

Mr. Ila Pal is VP of Marketing at Ironwood Electronic, USA. He holds a MS degree in Mechanical Engineering from Iowa State University, Ames, USA. He holds a MBA degree from University of St. Thomas, Minneapolis, USA. He has six patents relating to high performance BGA socket design. He has presented many papers related to interconnection technology and published articles in reputed journals. He has spent more than 15 years developing new technologies in the Packaging and Interconnection field. He can be reached at ila@ironwoodelectronics.com


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